We claim:

1. A process for making an integrated circuit, comprising:

a) providing a substrate or epitaxial layer of p-type material; and

b) applying a sequence of mask steps as follows:

(1) applying a first mask and forming at least one N-well in said p-type material therethrough;

(2) applying a second mask and forming an active region therethrough;

(3) applying a third mask and forming a p-type field region therethrough;

(4) applying a fourth mask and forming a gate oxide therethrough;

(5) applying a fifth mask and carrying out a p-type implantation therethrough;

(6) applying a sixth mask and forming polysilicon gate regions therethrough;

(7) applying a seventh mask and forming a p-base region therethrough;

(8) applying an eighth mask and forming a N-extended region therethrough;

(9) applying a ninth mask and forming a p-top region therethrough;

(10) applying a tenth mask and carrying out an N+ implant therethrough;

(11) applying an eleventh mask and carrying out a P+ implant therethrough;

(12) applying a twelfth mask and forming contacts therethrough;

(13) applying a thirteenth mask and depositing a metal layer therethrough;

(14) applying a fourteenth mask and forming vias therethrough;

(15) applying a fifteenth mask and depositing a metal layer therethrough; and

(16) applying a sixteenth mask and forming a passivation layer therethrough; and

wherein up to any three of mask steps 4, 7, 8, and 9 may be omitted depending on the type of integrated circuit.

2. A process as claimed in claim 1, comprising mask steps 1, 2, 3, 5, 6, 8, 10, 11, 12, 13, 14, 15, and 16.

3. A process as claimed in claim 1, comprising mask steps 1, 2, 3, 5, 6, 9, 10, 11, 12, 13, 14, 15, and 16.

4. A process as claimed in claim 1, comprising mask steps 1, 2, 3, 5, 6, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

5. A process as claimed in claim 1, comprising mask steps 1, 2, 3, 5, 6, 7, 10, 11, 12, 13, 14, 15, and 16.

6. A process as claimed in claim 1, comprising mask steps 1, 2, 3, 5, 6, 7, 8, 10, 11, 12, 13, 14, 15, and 16.

7. A process as claimed in claim 1, comprising mask steps 1, 2, 3, 5, 6, 7, 9, 10, 11, 12, 13, 14, 15, and 16.

8. A process as claimed in claim 1, comprising mask steps 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

9. A process as claimed in claim 1, comprising mask steps 1, 2, 3, 4, 5, 6, 10, 11, 12, 13, 14, 15, and 16.

10. A process as claimed in claim 1, comprising mask steps 1, 2, 3, 4, 5, 6, 9, 10, 11, 12, 13, 14, 15, and 16.

11. A process as claimed in claim 1, comprising mask steps 1, 2, 3, 4, 5, 6, 9, 10, 11, 12, 13, 14, 15, and 16.

12. A process as claimed in claim 1, comprising mask steps 1, 2, 3, 4, 5, 6, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

13. A process as claimed in claim 1, comprising mask steps 1, 2, 3, 4, 5, 6, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

14. A process as claimed in claim 1, comprising mask steps 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, and 16.

15. A process as claimed in claim 1, comprising mask steps 1, 2, 3, 4, 5, 6, 7, 8, 10, 11, 12, 13, 14, 15, and 16.

16. A process as claimed in claim 1, comprising mask steps 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, and 16.

17. A process as claimed in claim 1, comprising mask steps 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

18. A process as claimed in claim 1, wherein each mask step is associated with several sub-process steps.

19. A method as claimed in claim 1, wherein each mask step is associated with the sub-process steps set forth in the following table:

Mask No.	Sub-Process Steps
Mask 1: N-Well	Starting Material : P- Bulk Silicon
	Oxidation (Initial oxide)
	Photo
	N-Type Implant (N-Well)
	Diffusion
Mask 2: Active Area	Oxide Etch
	Oxidation (Subnitox)
	Silicon Nitride Deposition (CVD)
	Photo
	Nitride Etch
Mask 3: P-Field	Photo
	P-Type Implant (P-Field)
	Blanket N-Type Implant (N-Field)
	Oxidation (Field Oxide)
	Nitride Etch
	Oxide Etch
	Oxidation (Pre-Gate Oxide)
Mask 4: High-voltage Gate Oxide	Oxide Etch
	Oxidation (High-voltage Gate Oxide)
	Photo
Mask 5: Thin Gate oxide & VTP Adjust	Oxide Etch
	Oxidation (Thin Gate Oxide)
	Photo
	P-Type Implant (VTP Adjust)
Mask 6: Polysilicon Gate Patterning	Polysilicon Gate Deposition (CVD)
	Polysilicon Doping
	Photo
	Polysilicon Etch
Mask 7: P-Base	Photo
	P-Type Implant (P-Base)
Mask 8: N-Extended	Photo
	N-Type Implant (N-Extended)
Mask 9: P-Top	Photo
	P-Type Implant (P-Top)
Mask 10: N+ Implant	Oxidation and Diffusion
	Polysilicon Oxidation
	Photo
	N-Type Implant (N+)
Mask 11: P+ Implant	Photo
	P-Type Implant (P+)
Mask 12: Contacts	SG/PSG/SOG (Oxide) Deposition
	Diffusion
	Photo

	Contact Etch
Mask 13: Metal 1	Ti/TiN Deposition with Oxidation
	Aluminium Alloy Deposition
	Photo
	Metal Etch
	Dielectric and SOG (Oxide) Deposition
Mask 14: Vias	Photo
	Vias Etch
Mask 15: Metal 2	Ti/TiN Deposition with Oxidation
	Aluminium Alloy Deposition
	Photo
	Metal Etch
	Oxide / Nitride Deposition
Mask 16: Passivation	Photo
	Oxide Etch